# Circuit-Averaged Modeling of Non-Ideal Low-Power DC-AC Inverters

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***Abstract*—With the growing demand for electrical DC storage and sources, DC-AC conversion has become an indispensable component for not only high and medium, but also low-power applications. This paper introduces an efficient and accurate multi-harmonic circuit-averaged modeling technique for non-ideal pulse-width modulated DC-AC inverters for low-power applications. The proposed model significantly reduces simulation times by using circuit-averaging and accurately anticipates the AC signal response by modeling the circuit behavior at different harmonics. The proposed model deploys the inductor current in the filter at the inverter output as a state variable, and accurately records circuit dynamics while accounting for switching losses associated with non-ideal devices. We show that the developed index-0 and index-1 circuits compare well with transistor-level simulations under a variety of operating conditions.**

## I. Introduction

The transient and steady-state simulations of non-linear power electronic converters has traditionally been very computationally expensive due to the presence of non-ideal switching devices that must be simulated with small time resolutions and a large number of harmonics to accurately capture the dynamic behavior of the converter. Several approaches in the literature have been presented to improve the efficiency of simulations without compromising the accuracy of the results, such as using the circuit-averaging technique for DC-DC converters [1]. In addition, frequency-dependent averaged models for Pulse-Width Modulated (PWM) DC-DC converters have been developed using multi-harmonic averaging techniques to improve the accuracy of the simulations [2], [3], [4], [5]. These models capture the effects of higher order harmonics while preserving the computational efficiency of averaged models. More recently, a generalized model that can be applied to any DC-DC converter, has been presented that combines the accuracy of state-space averaging, the flexibility of PWM switch models and the multi-frequency nature of the averaging technique in [6], [7]. Nevertheless, these methods were all developed exclusively for DC-DC converters.

DC-AC converters, more commonly referred to as inverters, remain the cornerstone of DC-supplied energy sources [8], [9]. The fact that most grids and many electrical appliances are AC signal dependent makes it impossible to exclusively rely on circuits that strictly use DC signals. Furthermore, the recent emergence of technologies such as modern electric vehicles and photovoltaic micro-inverter systems has resulted in an increase in the use of low-power DC-AC inverters [10]. Unfortunately, the simulation and modeling of low power DC-AC inverters has not been properly addressed in the literature. Furthermore, the use of conventional circuit-averaged based techniques on DC-AC inverter circuits was not possible since those models focus exclusively on modeling the DC behavior, and any AC waveforms are assumed to be small. Such assumptions are insufficient in the case of inverters [11].

In this paper, we utilize the multi-harmonic averaging technique, first introduced in [6], to produce for the first time a generalized and equivalent circuit-averaged model that would properly estimate the output waveforms of DC-AC inverters while reducing the simulation time. Our proposed model accounts for the unique characteristics of inverters, namely the PWM switching function and the large-signal variations in the waveforms. The model is tested on a common MOSFET H-bridge inverter used to convert low power DC signals to AC sine wave signals. The original circuit model is averaged at different orders, thereby removing the switching components in the equivalent circuit model. Our proposed model generates the calculated responses and accurately captures the most significant harmonic orders efficiently. In this paper, we focus on the index-0 and index-1 circuits, which are the dominant components on the output spectrum of a typical sine wave inverter. In summary, this work presents the following new technical contributions:

- Equivalent averaged circuit models for the first order characterization of the output waveforms of a H-bridge MOSFET DC-AC inverter circuit.
- The expressions for calculating the dc and first order series expansions for the currents and voltages at the inverter output in addition to the switching waveform.
- The output waveforms are obtained with a computation time that is up to one order of magnitude faster than through transistor-level simulation, with an accuracy loss below 4%.

The remainder of the paper is organized as follows. Section II gives an overview of the characteristics and operation of

DC-AC inverters. Section III presents an overview of the large-signal averaged modeling technique in power electronic converters. Section IV presents the proposed index-0 and index-1 averaged models for inverters. Numerical simulation results are shown in section V to demonstrate the accuracy and efficiency of using the proposed model followed by the conclusion in section VI.

## II. Overview of DC-AC inverter operation

Generating a centered sine wave from a DC signal requires passing both positive and negative voltages across a load. Four MOSFET switches in an H-bridge configuration are capable of this transformation. In the example circuit of Fig. 1, four n-channel MOSFETs are used to minimize power loss and exploit higher switching speeds. There are four possible transistor states during operation as follows:

- M1 on, M3 on; $V_{out} = V_{in}$
- M1 on, M4 on; $V_{out} = 0$
- M2 on, M4 on; $V_{out} = -V_{in}$
- M2 on, M3 on; $V_{out} = 0$

We can summarize the switching condition using a switching function, $q(t)$, defined as:

$$q(t) = \begin{cases} 1 & V_{out} = V_{in} \\ 0 & V_{out} = 0 \\ -1 & V_{out} = -V_{in} \end{cases} \tag{1}$$

The general switching function can be defined over one switching cycle as shown in Fig. 2 and the relations below:

$$q(t) = \begin{cases} 0 & t \in [0, \delta] \\ 1 & t \in [\delta, dT_s - \delta] \\ 0 & t \in [dT_s - \delta, dT_s + \delta] \\ -1 & t \in [dT_s + \delta, T_s] \\ 0 & t \in [T_s, T_s + \delta]) \end{cases} \tag{2}$$

In (2), $\delta$ is the rise/fall time delay, $d$ is the duty cycle of the switching signal, and $T_s$ is the switching period.

## III. Overview of Circuit-Averaging

In this section, an overview of the multi-harmonic circuit averaging technique is presented. The general signal waveform $x(\tau)$ can be described over the interval $\tau \in [t-\tau, t]$ by the Fourier series,

$$x(\tau) = \sum_{k=-\infty}^{k=+\infty} \langle x \rangle_k \, e^{jk\omega_s \tau} \tag{3}$$

where $\omega_s = 2\pi/T_s$ and $T_s$ is the switching period. $\langle x_k \rangle (t)$ are the Fourier Series coefficients as a function of time, which can be represented as:

$$\langle x \rangle_k (t) = \int_{t-\tau}^{t} x(\tau) e^{-jk\omega_s \tau} dt \tag{4}$$

In (3), the $k^{th}$ coefficient of the Fourier series is referred to as the index-k average i.e. $\langle x \rangle_0 (t)$ represents the index-0 component, and $\langle x \rangle_1 (t)$ denotes index-1, or the first harmonic, etc. $x(\tau)$ can therefore be expressed as:

$$x(\tau) = \langle x \rangle_0 + 2 \sum_{l=1}^{\infty} (\Re(\langle x \rangle_l) \cos(l\omega_s \tau) - \Im(\langle x \rangle_l) \sin(l\omega_s \tau)) \tag{5}$$

In (5), $\Re(\langle x \rangle_l)$ and $\Im(\langle x \rangle_l)$ signify the real and imaginary parts of $\langle x \rangle_l$ respectively and the factor of 2 is due to the symmetry of the $k$ index in (3) from $-\infty$ to $+\infty$. It is important to note that the higher the order of harmonics that is used, the more accurate the model becomes at capturing the switching behavior. However, note that the Fourier transform of a typical sine wave DC-AC inverter shows that the voltage response is dominated by the dc and first order component under typical operating conditions, as shown in Fig. 3. For this purpose, we will focus on the development of the index-0 and index-1 averages in this paper due to space limitation, although there will be cases where the index-1 model will not be sufficient, such as for non-sine wave inverters.

## IV. DC-AC Inverter Averaged Model

In this section, we show how circuit averaging can be applied to DC-AC inverters. We will focus on deriving the expressions for the index-0 and index-1 models of the circuit of Fig.1, where the inductor current acts as a state-variable.

### A. Multi-Harmonic Averaging of the Inverter Circuit

In order to properly capture the behavior of the inverter and successfully apply the averaging technique, relations for both the output current and voltage need to be derived. Applying Kirchhoff's voltage law (KVL) to the circuit of Fig. 1 while assuming ideal switches yields the equation:

$$\frac{di(t)}{dt} = \frac{1}{L}(\underbrace{qV_{in}}_{V_{out}} - v(t)) \tag{6}$$

where $V_{out}$ is equal to $qV_{in}$, the switching function multiplied by the input voltage. From equation (6), we can find the index-0 relation:

$$\frac{d \langle i \rangle_0}{dt} = \frac{1}{L}(\langle qV_{in} \rangle_0 - \langle v \rangle_0) \tag{7}$$

The index-1 inductor current state variable relation is defined as [2]:

$$\frac{d \langle i \rangle_1}{dt} = -jw_s \langle i \rangle_1 + \frac{1}{L}(\langle qV_{in} \rangle_1 - \langle v \rangle_1) \tag{8}$$

We can now expand $\langle qV_{in} \rangle_0$ and $\langle qV_{in} \rangle_1$ in equations (7) and (8) to give the following:

$$\begin{aligned} \frac{d \langle i(t) \rangle_0}{dt} = \frac{1}{L}(&\langle q \rangle_0 \langle V_{in} \rangle_0 + 2 \langle q \rangle_1^R \langle V_{in} \rangle_1^R \\ &+ 2 \langle q \rangle_1^I \langle V_{in} \rangle_1^I - \langle v \rangle_0) \end{aligned} \tag{9}$$

$$\begin{aligned} \frac{d \langle i(t) \rangle_1}{dt} = -jw_s \langle i \rangle_1 + \frac{1}{L}(&\langle q \rangle_0 \langle V_{in} \rangle_1 + j \langle q \rangle_0 \langle V_{in} \rangle_1 \\ &+ \langle q \rangle_1 \langle V_{in} \rangle_0 + j \langle q \rangle_1 \langle V_{in} \rangle_0 - \langle v \rangle_1) \end{aligned} \tag{10}$$

Where the superscripts $R$ and $I$ signify the real and imaginary components respectively. We can simplify equations (9) and

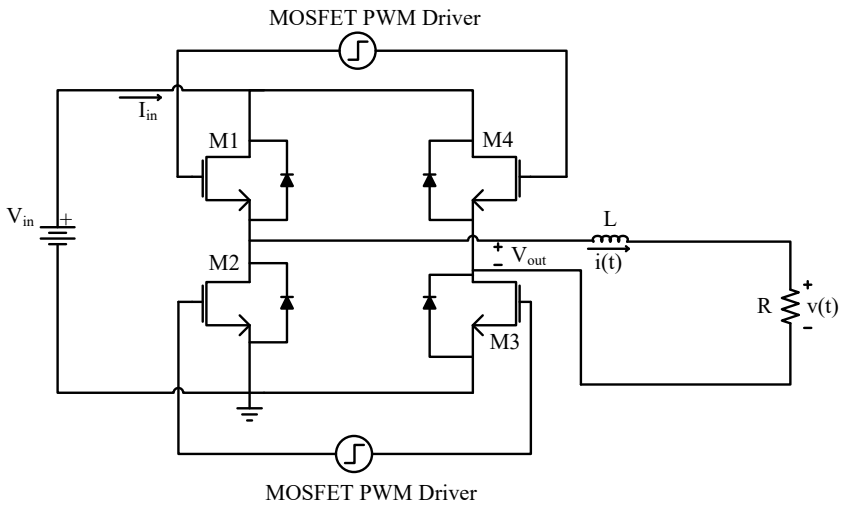


Fig. 1. NMOS H-Bridge Inverter

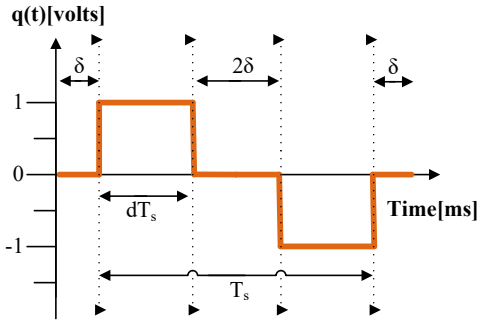


Fig. 2. Switching signal q(t)

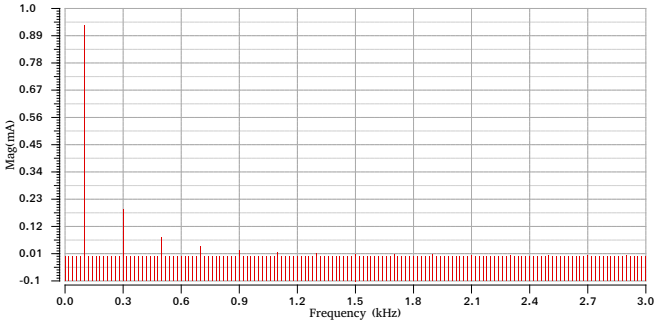


Fig. 3. Fourier Transform of DC-AC inverter inductor output current

(10) by noting that $V_{in}$ has only a DC component. In this case we have:$\langle V_{in}\rangle_1 = 0$; $V_{in} = \langle V_{in}\rangle_0$;$\langle V_{in}\rangle^I = 0$. Equations (9) and (10) would then simplify to:

$$\frac{d\langle i\rangle_0}{dt} = \frac{1}{L}(\langle q\rangle_0 V_{in} - \langle v\rangle_0) \tag{11}$$

$$\frac{d\langle i\rangle_1}{dt} = -jw_s\langle i\rangle_1 + \frac{1}{L}(\langle q\rangle_1 V_{in} + j\langle q\rangle_1 V_{in} - \langle v\rangle_1) \tag{12}$$

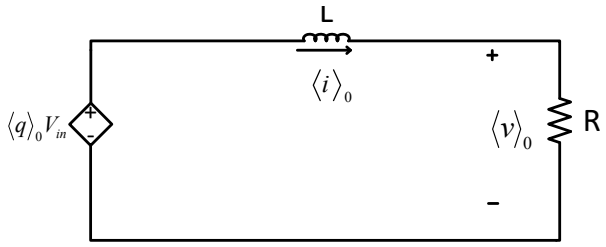


Fig. 4. Index-0 simplified inverter average model

For the index-1 relation in (12), we can seperate the real and imaginary components, which will give:

$$\frac{d\langle i\rangle^R_1}{dt} = w_s\langle i\rangle^I_1 + \frac{1}{L}(\langle q\rangle^R_1 V_{in} - \langle v\rangle^R_1) \tag{13}$$

$$\frac{d\langle i\rangle^I_1}{dt} = -w_s\langle i\rangle^R_1 + \frac{1}{L}(\langle q\rangle^I_1 V_{in} - \langle v\rangle^I_1) \tag{14}$$

Using equations (11), (13), and (14) we can develop the multi-harmonic averaged matrix of the inverter coupled with a resistive-inductive filter as follows:

$$\frac{d}{dt}\begin{bmatrix}\langle i\rangle_0\\ \langle i\rangle^R_1\\ \langle i\rangle^I_1\end{bmatrix} = \begin{bmatrix}\frac{\langle q\rangle_0}{L}\\ \frac{\langle q\rangle_0 R}{L}\\ \frac{\langle q\rangle^R_1}{L}\\ 0\\ 0\\ 0\end{bmatrix} V_{in} + \begin{bmatrix}0 & 0 & -\frac{1}{L} & 0 & 0 & 0\\ 0 & 0 & 0 & w_s & -\frac{1}{L} & 0\\ 0 & -w_s & 0 & 0 & 0 & -\frac{1}{L}\end{bmatrix}\begin{bmatrix}\langle i\rangle_0\\ \langle v\rangle_0\\ \langle i\rangle^R_1\\ \langle i\rangle^I_1\\ \langle v\rangle^R_1\\ \langle v\rangle^I_1\end{bmatrix} \tag{15}$$

These equations map to index 0 and 1 circuits represented in Fig. 4 and Fig. 5.

### *B. Accounting for Losses in the Average Model*

For additional accuracy, the switching losses will have to be taken into consideration. Two resistors, $r_1$ and $r_2$, can be added to the model to simulate the voltage drops due to the non-ideal switches in the circuit. We can then deduce the index-0 and

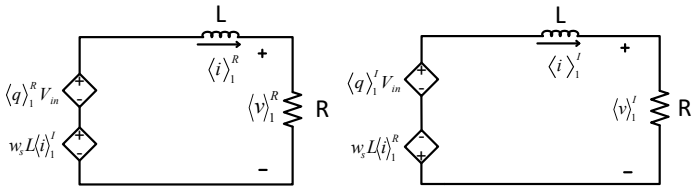


Fig. 5. Index-1 simplified inverter average model

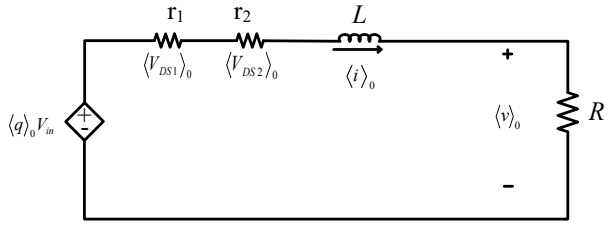


Fig. 6. Index-0 simplified inverter average model

index-1 expressions from equations (11), (13), and (14) while accounting for the drain-to-source voltage drops across the two operating transistors, which we will refer to as $V_{DS1}$ and $V_{DS2}$. More specifically, we can express the voltage across the inductor as:

$$\frac{di}{dt} = \frac{1}{L}(qV_{in} - V_{DS1} - V_{DS2} - V_R) \tag{16}$$

Then, at index-0 with the expansion of $\langle qV_{in}\rangle_0$ from [6] and [2] and $\langle V_{in}\rangle = 0$ as previously mentioned, we obtain:

$$\frac{d\langle i\rangle_0}{dt} = \frac{1}{L}(\langle q\rangle_0 V_{in} - \langle V_{DS1}\rangle_0 - \langle V_{DS2}\rangle_0 - \langle V\rangle_0) \tag{17}$$

For the index-1 current flowing through the inductor, we can express the equations using real and imaginary components as follows:

$$\frac{d\langle i\rangle_1^R}{dt} = w_s L\langle i\rangle_1^I + \langle q\rangle_1^R V_{in} - \langle V_{DS1}\rangle_1^R - \langle V_{DS2}\rangle_1^R - \langle V\rangle_1^R) \tag{18}$$

$$\frac{d\langle i\rangle_1^I}{dt} = -w_s L\langle i\rangle_1^R + \langle q\rangle_1^I V_{in} - \langle V_{DS1}\rangle_1^I - \langle V_{DS2}\rangle_1^I - \langle V\rangle_1^I) \tag{19}$$

From equations (17), (18), and (19) we are able to produce both index 0 and 1 equivalent average models, as shown in Fig. 6 and Fig. 7, respectively. Note that the resistor values for $r_1$ and $r_2$ are evaluated in real-time using simulation based device characterization [12], which allows for accurate and automated computation of the transistor voltage drops $V_{DS}$, which are nonlinear functions of the circuit state and will vary dynamically during the circuit simulation. These can be evaluated without simulating the actual converter as explained in [12]. In summary, the evaluation of the voltage drop $V_{DS}$ is achieved by adding an additional circuit which is constructed such that an additional non-switching transistor has the same bias as the transistor in the inverter circuit to ensure that the voltage drop produced across it is the same as that in the inverter. Returning the voltage drop to the equivalent model allows the model to account for this type of non-ideality. Similar procedures can be applied to account for other device losses. It is important to note that the additional transistor uses the same device model (e.g. BSIM3/4), thus the behavior captured fully accounts for the device non-idealities of the transistors in the original circuit.

Next, we show how to compute the index-k average of the switching function $q(t)$.

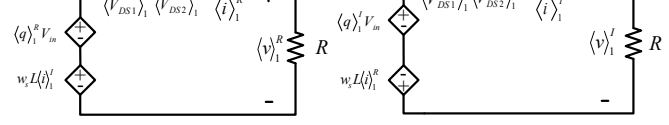


Fig. 7. Index-1 simplified inverter average model

### C. Averaging of Inverter Switching Function

Using the switching boundaries in (2), Fig. 2 and in (4), the index-0 and index-1 averages of $q(t)$ can be calculated accordingly:

$$\langle q\rangle_k(t) = \frac{1}{T_s}\int_{\delta}^{T_s} q(\tau)e^{-jkw_s\tau}dt \tag{20}$$

Consequently solving for $q(t)$ at index $k = 0$ results in:

$$\langle q\rangle_0 = 2d - 1 \tag{21}$$

Likewise, solving for $q(t)$ at index $k = 1$ results in:

$$\begin{aligned}\langle q\rangle_1 = -\frac{1}{j\omega_s T_s}[&\cos(\omega_s(dT_s-\delta)) - j\sin(\omega_s(dT_s-\delta))\\ &- \cos(\omega_s\delta) + j\sin(\omega_s\delta) - \cos(\omega_s T_s) + j\sin(\omega_s T_s)\\ &+ \cos(\omega_s(dT_s+\delta)) - j\sin(\omega_s(dT_s+\delta))]\end{aligned} \tag{22}$$

The relations in (21) and (22) are used to determine the coefficients required in the equivalent models in Fig. 6 and Fig. 7. Next we show the results of some numerical simulations to demonstrate the accuracy and the efficiency of using the proposed model.

## V. Numerical Examples

The proposed circuit-averaged model for DC-AC inverters was tested on the inverter circuit in Fig. 1 under the variety of operating conditions, or scenarios, described in Table I. Note that the values of the resistance $R = 10k\Omega$ and the inductance $L = 10H$ in all four scenarios. The proposed equivalent circuits of Fig. 4 and Fig. 5 were implemented in Cadence using Verilog-A and the standard analog library. The results were bench-marked against the transistor level simulations using Spectre running on a Cadence workstation and CMOS $18\mu m$ technology. The different scenarios are selected to show the flexibility and robustness of the model. Note that in scenario IV, a duty ratio of 20% is selected for the switching function, which naturally produces a heavily distorted waveform at the output of the inverter that is far

from resembling a sine wave. In such a scenario, higher order harmonic indexes need to be accounted for to accurately reproduce the waveform. However, we have still selected this scenario to show the accuracy of the index-0 and index-1 components under different duty cycle conditions.

### A. Accuracy Comparison

The inductor current waveforms of the transistor circuit, the average circuits and reconstructed waveform operating under the conditions of scenarios I, II and III are shown in Fig. 8. Note that the results of the proposed model assume ideal switches (i.e. the least accurate, worst-case, comparison). Furthermore, as can be seen, the output waveforms of the selected transistor circuit exhibit some distortion from a pure sinusoid and therefore contain some higher order harmonics. As can be seen, the results compare very well, especially given the fact that only the first harmonic is accounted for in our model. This is verified in the numerical results of the simulation shown in Table II, which directly compare the values of the first harmonic in the original circuit waveform with those obtained using the proposed model. For scenario IV, due to the $20\%$ duty ratio, the output waveform of the original switching circuit is significantly distorted from a sinusoidal AC waveform, and in this case, the index-1 averaged circuit is not sufficient to accurately reproduce the output waveform. However, even in this scenario, a comparison of the first harmonic amplitude in Table II verifies the accuracy of our proposed model.

### B. Computation Cost Comparison

The speed-up in running a transient simulation was significantly improved using our proposed average model as shown in Table III. It is important to note that speed-up will vary depending on the length of the transient simulation and our CPU time comparison was selected based on a conservative transient simulation of five time periods. In all cases, the proposed model simulation time will always be substantially faster. It is also important to mention that although the transient simulation of the original circuit is already quite fast, there is still a significant advantage in obtaining such speed-ups since practical integrated circuits need to account for robustness in the design and verification process. In industrial practice, methods such as Monte-Carlo analysis and other deterministic methods are commonly used for robustness analysis and typically require hundreds or thousands of simulations [13]. Such repeated simulations would typically have a long runtime. Therefore, methods to speed up the simulation can have a big impact on the design process.

## VI. Conclusion

In this paper, a true circuit-averaged model for PWM driven DC-AC inverters is proposed. The model is capable of predicting AC responses in addition to the DC average values by accounting for higher order harmonic effects. The equivalent circuits for the index-0 and index-1 averages are presented. The model was tested under different scenarios and the results were very accurate while presenting significant speed-up in simulation time.

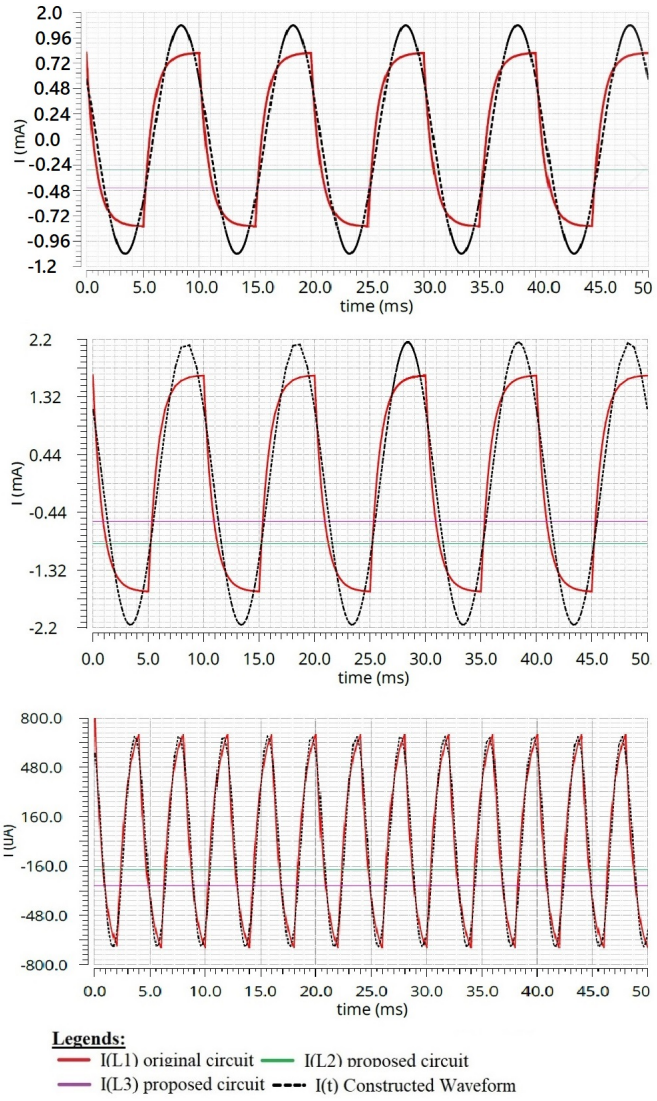


Fig. 8. Comparison of inductor current waveform between the original circuit and the proposed first order model of scenarios I, II and III

TABLE I
NUMERICAL EXAMPLE SCENARIO DESCRIPTIONS

| Scenario | $V_{in}[V]$ | Freq.[Hz] | duty ratio | $q_0$ | $q_1$ |
|---|---|---|---|---|---|
| **I** | 10 | 100 | 0.5 | 0 | -0.636j |
| **II** | 20 | 100 | 0.5 | 0 | -0.636j |
| **III** | 10 | 250 | 0.5 | 0 | -0.636j |
| **IV** | 10 | 100 | 0.2 | 0.6 | 0.302-0.22j |

## Acknowledgments

This work is supported by the Lebanese American University. The authors would also like to thank the Chair of Electronic Design Automation at the Technical University of

TABLE II
COMPARISON OF DC AND FIRST HARMONIC NUMERICAL RESULTS FOR THE INDUCTOR CURRENT

| Circuit | Variable | Scenario I | II | III | IV |
|---|---|---|---|---|---|
| Original | $\lvert I_0 \rvert [\mu A]$ | 0 | 0 | 0 | 600.6 |
| Proposed | $\lvert \langle I \rangle_0 \rvert [\mu A]$ | 0 | 0 | 0 | 601.2 |
| **% difference** | | **0.0%** | **0.0%** | **0.0%** | **0.1%** |
| Original | $\lvert I_1 \rvert [\mu A]$ | 1031.0 | 2167.5 | 657.0 | 606.1 |
| Proposed | $2 \times \lvert \langle I \rangle_1 \rvert [\mu A]$ | 1068.5 | 2154.2 | 682.1 | 632.0 |
| **% difference** | | **3.5%** | **0.6%** | **3.8%** | **4.2%** |

TABLE III
COMPUTATION TIME COMPARISON IN MILLISECONDS.

| Scenario | Original | Proposed | Speedup |
|---|---|---|---|
| **I** | 52.357 | 8.689 | 6.03x |
| **II** | 68.791 | 8.740 | 7.87x |
| **III** | 102.262 | 8.421 | 12.14x |
| **IV** | 53.332 | 8.885 | 6.00x |

Munich for allowing the use of their workstations to run Cadence.

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